

## **Semiconductor Device and Method of Fabricating the Same**

### **Cross Reference To Related Application**

#### **【0001】**

5       The present document is based on Japanese Priority Document JP2003-111437, filed in the Japanese Patent Office on April 16, 2003, the entire contents of which being incorporated herein by reference.

### **Background of the Invention**

#### **【0002】**

##### **1. Field of the Invention**

15       The present invention relates to a semiconductor device and a method of fabricating such semiconductor device, and more specifically to a semiconductor device having a multilevel interconnection for electrically connecting a plurality of conduction layers through connection holes formed in an insulation layer and a method of fabricating such a semiconductor device.

#### **【0003】**

##### **2. Description of Related Art**

25       With the development of higher integration density and performance of LSIs (Large Scale Integrated Circuits), device dimensions are increasingly miniaturized and devices are multi-layered. In order to reduce ever increasing wiring delay due to miniature multi-layered wiring, it is necessary to scale with appropriate ratios such parameters, for example, wiring film thickness which affect wiring resistance and capacity, a film thickness  
30       between layers and a relative dielectric constant which affect wiring capacitance, and a wiring resistivity which

affects wiring resistance and the like.

【0004】

As for wiring materials, it is preferable to have a lower resistivity so as to transmit electrical signals without large voltage drop. Metals like gold (Au), copper (Cu) and silver (Ag) exhibit lower resistivity than aluminum (Al) which has been widely used. It is reported that among other metals, copper has a higher melting point than aluminum and higher activation energy to cause the electro-migration phenomenon, thereby improving reliability as compared to aluminum. However, in order to use copper as miniature wiring, since there is no suitable gas to perform dry etching on the insulation film having a copper underlayer with high selectivity ratio, buried wiring is generally formed by utilizing the Damascene technique. In particular, the dual-damascene technique in which both connection holes and wiring are buried is effective from the viewpoints of expanding alignment margin in lithography and shortening fabrication processing.

【0005】

Also, it is preferable that an insulation layer has a smaller relative dielectric constant in order to reduce wiring capacitance. Materials to be used are shifting to a low relative dielectric constant materials represented by allyl ether resin, SiOC and the like. However, the low relative dielectric constant materials such as allyl ether resin have lower Young's modulus than a SiO<sub>2</sub> film or SiO<sub>2</sub> film containing fluorine used in the related art, thereby providing relatively less dense films.

【0006】

FIG. 10 is a diagrammatic cross section view of a part of a semiconductor device in the related art. An insulation film 2 is formed on the upper surface of a semiconductor substrate 1. Formed on a part of the upper surface of the insulation film 2 are wiring grooves in which a first conductive layer 3 and a second conductive layer 4 are formed. A diffusion protection film 5 is formed on the upper surface of the insulation film 2 on which the first conductive layer 3, and the second conductive layer 4 are formed and an insulation film 6 is formed on the upper surface of the diffusion protection film 5. A third conductive layer 8 is formed in a wiring groove which is formed on a part of the upper surface of the insulation film 6. A diffusion protection film 9 is formed on the insulation film 6 on which the third conductive layer 8 is formed. An insulation film 10 is formed on the upper surface of the diffusion protection film 9. Additionally, the first conductive layer 3, the second conductive layer 4 and the third conductive layer 8 are electrically interconnected by way of opening portions 7. It is to be noted here that the same material as the third conductive layer 8 is filled in the opening portions. The diffusion protection films 5, 9 may be eliminated depending on the layer structure and the material of the conductive layers. Device areas and device isolation areas to be formed on the semiconductor substrate 1 are not shown in the drawing.

【0007】

As a method of fabricating a semiconductor device as described hereinabove, it is known to form an



wiring in the subsequent high temperature processing steps such as forming an upper layer insulation film, curing or the like. Opening portions are normally formed at end portions of the conductive layers for making  
5 electrical connection with the underlying wiring. If it is designed to apply a fixed potential, thereby not flowing a large current through the opening, only one opening portion is formed. Accordingly, the upper section of the opening portion 7 is stretched in the  
10 direction of the longer length of the third conductive layer 8 when it expands by thermal expansion, thereby peeling the less closely attached connection portion, i.e., at the interface between the bottom portion of the connection hole 7 and the lower wiring layer (namely,  
15 the first conductive layer 3 and the second conductive layer 4 in FIG. 10 and FIG. 11). This means that the connection hole 7 becomes an electrically isolated conductive layer 20. As described above, in the related art, since deformation, disconnection or the like occurs  
20 at connection portions between particularly fragile wiring, it is most likely that production yield and wiring reliability are largely affected.

#### 【0010】

In consideration of the above circumstances, the  
25 present invention provides a semiconductor that enables to suppress deformation of the opening portions due to thermal expansion and contraction and to improve production yield and reliability wiring, and a method of fabricating such semiconductor device.

#### 30 【0011】

In order to address the above, the semiconductor

device according to the present invention includes a substrate, a first conductive layer formed on the substrate, a second conductive layer formed on the substrate at a predetermined distance from the first conductive layer, an insulation film formed on the upper surfaces of the first conductive layer and the second conductive layer and having a plurality of first opening portions to expose either the first conductive layer or the second conductive layer and second opening portions to expose neither the first conductive layer nor the second conductive layer, and a third conductive layer formed on the upper surface of the insulation film in such a manner to fill up the first opening portions and the second opening portions and to make electrical connection with the first conductive layer and the second conductive layer by way of the first opening portions, wherein the second opening portions are formed between a pair of the first opening portions along the third conductive layer.

20    **【0012】**

          In the semiconductor device according to the present invention as defined hereinabove, the second opening portions are formed between a pair of the first opening portions along the third conductive layer, thereby dispersing any force to be applied to the first opening portions and suppressing any deformation of the first opening portions which are the connection portions between the third conductive layer and either the first conductive layer or the second conductive layer.

30    **【0013】**

          The semiconductor device according to the present

invention includes a substrate, a first conductive layer formed on the substrate, a second conductive layer formed on the substrate at a predetermined distance from the first conductive layer, an insulation film formed on the upper surfaces of the first conductive layer and the second conductive layer and having opening portions to expose either the first conductive layer or the second conductive layer, and a third conductive layer formed on the upper surface of the insulation film in such a manner to fill up the opening portions and to make electrical connection with the first conductive layer and the second conductive layer, wherein the third conductive layer has a predetermined wiring length to maintain electrical connection even if the length in the direction of the longer length is thermally expanded or contracted and also makes electrical connection with the first conductive layer and the second conductive layer by way of the opening portions.

【0014】

In the semiconductor device as defined hereinabove, third conductive layers has a predetermined wiring length so that electrical connection with the first conductive layers and the second conductive layers is maintained by way of the opening portions even if the length in the direction of the longer length thermally expanded or contracted.

【0015】

A method of fabricating a semiconductor device according to the present invention includes the steps of: forming a first conductive layer on a substrate; forming a second conductive layer on the substrate at

a predetermined distance from the first conductive layer;  
forming an insulation film on the upper surfaces of the  
first conductive layer and the second conductive layer;  
forming in the insulation film a plurality of first  
5 opening portions to expose either the first conductive  
layer or the second conductive layer and second opening  
portions to expose neither the first conductive layer  
nor the second conductive layer; and forming a third  
conductive layer on the upper surface of the insulation  
10 film in such a manner to fill up the first opening portions  
and the second opening portions and to make electrical  
connection with the first conductive layer and the second  
conductive layer; wherein the second opening portions  
is formed between a pair of the first opening portions  
15 along the third conductive layer.

【0016】

In the method of fabricating the semiconductor device  
according to the present invention, the first conductive  
layer is formed on the substrate and the second conductive  
20 layer is formed on the substrate at a predetermined  
distance from the first conductive layer. The  
insulation film is formed on the upper surfaces of the  
first conductive layer and the second conductive layer  
and is formed with a plurality of the first opening  
25 portions to expose either the first conductive layer or  
the second conductive layer and second opening portions  
to expose neither the first conductive layer nor the  
second conductive layer. The third conductive layer is  
formed on the upper surface of the insulation film to  
30 fill up the first opening portions and the second opening  
portions and to make electrical connection with the first



conductive layer and the second conductive layer by way of the first opening portions. It is to be noted that the second opening portions are formed between a pair of the first opening portions along the third conductive layer.

5      **【0017】**

A method of fabricating a semiconductor device according to the present invention includes the steps of: forming a first conductive layer on a substrate; forming a second conductive layer on the substrate at a predetermined distance from the first conductive layer; forming an insulation film on the upper surfaces of the first conductive layer and the second conductive layer; forming opening portions in the insulation film to expose either one end of the first conductive layers or of the second conductive layer; and forming a third conductive layer on the upper surface of the insulation film to fill up the opening portions and to make electrical connection with the first conductive layers and the second conductive layers; wherein the wiring length of the third conductive layer is made to a predetermined length to maintain connection even if the length in the direction of the longer length may vary due to thermal expansion or contraction and the third conductive layer makes electrical connection with the first conductive layers and the second conductive layers by way of the opening portions at both ends of the third conductive layer.

25      **【0018】**

In the method of fabricating the semiconductor device according to the present invention, the first conductive layer is formed on the substrate and the second conductive

layer is formed on the substrate at a predetermined distance from the first conductive layer. The insulation film is formed on the upper surfaces of the first conductive layer and the second conductive layer and the opening portions are formed in the insulation film to expose end portion of either the first conductive layer or the second conductive layer. The third conductive layer is formed on the upper surface of the insulation film to fill up the opening portions and to make electrical connection with the first conductive layer and the second conductive layer. It is to be noted that the third conductive layer has a predetermined wiring length to maintain electrical connection even if the length in the direction of the longer length may vary due to thermal expansion or contraction and the third conductive layer makes electrical connection with the first conductive layer and the second conductive layer by way of the opening portions at both end portions of the third conductive layer.

20    **【0019】**

The semiconductor device according to the present invention is possible to suppress deformation at the opening portions due to thermal expansion and contraction of the conductive layers, thereby improving production yield and wiring reliability. Also, the method of fabricating the semiconductor device according to the present invention is possible to suppress deformation at the opening portions due to thermal expansion and contraction of the conductive layers, thereby improving production yield and wiring reliability.

## Brief Description of the Drawings

### 【0020】

In the drawings, FIG. 1 is a diagrammatic cross section view of a part of a semiconductor device according to a first embodiment of the present invention;

### 【0021】

FIG. 2A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention, and 2B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention;

### 【0022】

FIG. 3A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention and 3B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention;

### 【0023】

FIG. 4A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention and 4B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention;

### 30 【0024】

FIG. 5A is a diagrammatic cross section view

sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention and 5B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention;

【0025】

FIG. 6A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention and 6B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the first embodiment of the present invention;

【0026】

FIG. 7 is a diagrammatic cross section view of a part of the semiconductor device according to a second embodiment of the present invention;

【0027】

FIG. 8A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the second embodiment of the present invention and 8B is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the second embodiment of the present invention;

【0028】

FIG. 9A is a diagrammatic cross section view sequentially illustrating major steps of fabricating the semiconductor device according to the present invention and 9B is a diagrammatic cross section view sequentially

illustrating major steps of fabricating the semiconductor device according to the second embodiment of the present invention;

【0029】

5       FIG. 10 is a diagrammatic cross section view of a part of a semiconductor device in the related art; and

【0030】

FIG. 11 is a diagrammatic cross section view of a part of a semiconductor device in the related art.

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#### Description of Preferred Embodiments

【0031】

Next, preferred embodiments of the present invention will be described hereunder in greater detail by reference to the accompanying drawings.

15

<First Embodiment>

Next, a first embodiment of the present invention will be described by reference to FIG. 1. FIG. 1 is a diagrammatic cross section view of the semiconductor device according to the present embodiment of the present invention. An insulation film 102 is formed on a substrate 101. Wiring grooves 120 are formed in parts of the upper surfaces of the insulation film 102, and a first conductive layer 103 and a second conductive layer 104 made from, for example, Cu (i.e., copper) are formed in the wiring grooves 120 at a predetermined distance from each other. A diffusion protection film 105 is formed in such a manner to cover the first conductive layer 103 and the second conductive layer 104. Formed on the upper surface of the diffusion protection film 105 is an insulation layer 106 made from, for example,

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allyl ether resin having low Young's modulus. A wiring groove 125 is formed on the upper surface of the insulation film 106 in which a third conductive layer 108 made from, for example, Cu is formed. A diffusion protection film 109 and an insulation film 110 are sequentially formed on the upper surface of the insulation film 106 on which the third conductive layer 108 is formed. Also formed in the insulation film 106 is a plurality of first opening portions 107 in such a manner to expose either the first conductive layer 103 or the second conductive layer 104. The first conductive layer 103 and the second conductive layer 104 are electrically connected to the third conductive layer 108 by way of the first opening portions 107. Furthermore, second opening portions 111 are formed at a predetermined distance  $L_1$  between the pair of the first opening portions 107 along the third conductive layer 108 in such a manner not to expose the first conductive layer 103 or the second conductive layer 104. It is to be noted that the first opening portions 107 and the second opening portions 111 are filled with the same conductive material as the third conductive layer 108. Note that device areas, device isolation areas and the like which are formed in or on the substrate are not shown in the drawing for convenience.

## 25    【0032】

Next, a method of fabricating the semiconductor device according to the present invention will be described hereunder by reference to FIG. 2 - FIG. 6. FIG. 2 - FIG. 6 are diagrammatic cross section views sequentially illustrating major steps of fabricating the semiconductor device according to the present invention.

As shown in FIG. 2A, the insulation film 102 is formed on the upper surface of the semiconductor substrate 101 in which a certain device area is formed. On the upper surface of the insulation film 102, wiring grooves 120 having the depth  $t_1$ , are formed at, for example, two positions in the conductive layer forming area at a predetermined distance from each other by the existing lithography process, etching process or the like. In the present embodiment, the depth  $t_1$  is approximately 200 nm. The insulation film 102 is made from, for example, allyl ether resin. Subsequently, as shown in FIG. 2B, a barrier metal 121 is formed on the upper surface of the insulation film 102 having the wiring grooves 120 formed therein and then a first metal layer 122 is formed on the barrier metal 121. The barrier metal 121 is made from, for example, a tantalum (Ta) film of approximately 10 nm in thickness by sputtering process. On the other hand, the first metal layer 122 is made from an approximately 80 nm Cu seed film and approximately 700 nm Cu plating layer by electrolytic plating process.

【0033】

Then, as shown in FIG. 3A, the first metal layer 122 is polished by CMP (Chemical-Mechanical Polishing) process or the like until the insulation film 102 is exposed, thereby forming the first conductive layer 103 and the second conductive layer 104 in the wiring grooves 120. In the present embodiment, the first conductive layer 103 and the second conductive layer 104 are made from the same metal layer 122 but may be made from different metal layers. It is to be noted that the barrier metal is omitted in FIG. 3A and the subsequent drawings.

Subsequently, as shown in FIG. 3B, an approximately 50 nm thick SiC film is formed as the diffusion protection film 105 to prevent Cu from diffusing and also an approximately 600 nm thick insulation film 106 made from allyl ether resin or the like having a lower Young's modulus than the SiO<sub>2</sub> film is formed. The diffusion protection film 105 and the insulation film 106 are formed by choosing appropriate process depending on the materials used therefor.

10    【0034】

Then, as shown in FIG. 4A, the first opening portions 107 are formed in the insulation film 106 at the positions corresponding to end portions of the first conductive layer 103 and the second conductive layer 104 by the existing lithography process and etching process. Simultaneously, the second opening portions 111 are formed between the first opening portions 107 at a predetermined distance L<sub>1</sub> in the area where the third conductive layer 108 is to be formed but excluding the areas where the first conductive layer 103 and the second conductive layer 104 are formed. It is preferable that the diffusion protection film remains at the bottom of the first opening portions 107 and the second opening portions 111. The distance L<sub>1</sub> for forming the second opening portions 111 is determined depending on such factors as the wiring length of the third conductive layer 108 which will be formed later, Young's modules and coefficients of thermal expansion of the third conductive layer 108 and the insulation film 106, heating temperature in subsequent process and the like. In the present embodiment, the second opening portions 111 are formed



at every 100 $\mu$ m in the wire length of the third conductive layer 108. Then, as shown in FIG. 4B, a buried layer 123 is formed on the upper surface of the insulation film 106 in such a manner to fill out the first opening portions 107 and the second opening portions 111. A resist film 124 is formed on the upper surface of the buried layer 123 and the resist film 124 is processed by the existing lithography process in a predetermined pattern at the area where the third conductive layer 108 is formed.

10   【0035】

Next, referring to FIG. 5A, the buried layer 123 and the insulation film 106 excluding the area where the resist film 124 is formed are processed by the existing etching process. By removing the resist film 124 and the buried layer 123, a wiring groove 125 having the depth  $t_2$  is formed. Furthermore, the diffusion protection film 105 which is exposed to the first opening portions 107 and the second opening portions 111 is removed by etching process or the like, thereby exposing the first conductive layer 103 and the second conductive layer 104 to the first opening portions 107 and similarly exposing the underlying insulation film 102 to the second opening portions 111. In this present embodiment, the depth  $t_2$  of the wiring groove 125 is set to, for example, 300 nm. Then, referring to FIG. 5B, a barrier metal 126 and the second metal layer 127 are formed on the upper surface of the insulation film 106 in which the first opening portions 107, the second opening portions 111 and the wiring groove 125 are formed. The barrier metal 126 is formed from an approximately 20 nm thick Ta film by sputtering process. The second metal layer 127 is made

from, for example, an approximately 80 nm thick Cu seed film and an approximately 800 nm thick Cu film by electrolytic plating process or the like.

【0036】

5        Subsequently, as shown in FIG. 6A, the second conductive layer 127 and the barrier metal 126 are polished by the CMP process to expose the insulation film 106 in order to form the third conductive layer 108 having the barrier metal 126 and the second metal layer 127 only  
10    in the wiring groove 125. The third conductive layer 108 is not restricted to the aforementioned material but may be any conductive material containing copper. It is to be noted that the barrier metal 126 is omitted in FIG. 6A and the subsequent drawings. Next, referring  
15    to FIG. 6B, forming the diffusion protection film 109 and the insulation film 110 in the similar process, and further forming a conductive layer if desired, thereby forming multilevel interconnection. It is to be noted that the distance  $L_1$  and the number of the second opening  
20    portions 111 are not restricted to the aforementioned example but may vary depending on the film thickness of the conductive layers, dimensions of the opening portions, materials and film thickness of the insulation films, and the like. Also, the depth  $t_1$ ,  $t_2$  of the wiring grooves  
25    120, 125 may be varied depending on materials and film thickness of the insulation films.

【0037】

      In the present embodiment, the second opening portions 111 are formed at every 100 $\mu$ m between a pair  
30    of the first opening portions 107 which are formed in the third conductive layer 108. Allyl ether resin is

used as the insulation film 106. And Cu is used as the  
conductive layers, or the upper layer (the third  
conductive layer 108) and the lower layer (the first and  
second conductive layers 103, 104). The third  
5 conductive layer 108 is connected to the lower layer  
wiring 103, 104 by way of the first opening portions 107  
at both ends of the third conductive layer 108. Note  
that Young's modulus and coefficient of thermal expansion  
of Cu are 115 Gpa and 17.7 ppm/°C while those of allyl  
10 ether resin are 2.45 Gpa and 66 ppm/°C, respectively.  
Assuming that the conductive layers 103, 104 and 108 are  
formed to have a wiring length of, for example, 1000µm  
(repetitive configuration of a 1000µm upper conductive  
layer 108 and 1000µm lower conductive layers 103, 104)  
15 and the insulation film 106 which is made from allyl ether  
resin is formed between the upper and lower conductive  
layers. If the actual operating temperature is  
approximately 100°C, the aforementioned Young's modulus  
and coefficient of thermal expansion suggest that the  
20 wiring length expands approximately 800 nm per one end  
of the conductive layer. In other words, at the opening  
portions 107, an approximately 800 nm deforming force  
is applied from the lower conductive layers 103, 104 in  
one direction and similarly an approximately 800 nm  
25 deforming force is applied from the upper conductive layer  
in the opposite direction.

【0038】

In view of the 130 nm generation, since the diameter  
of the opening portions 107, 111 is approximately 200  
30 nm, a force enabling to deform the diameter equal to  
approximately 400% in the wiring direction is applied

from the upper and lower conductive layers, respectively, in the opposite directions. Accordingly, since the bottom portions of the first opening portions 107 and the underlying conductive layers 103, 104 are connected with insufficient adherence by way of the barrier metal and the like, it is easily understood that disconnection may occur. In case where the opening portions 107, 111 are formed in the third conductive layer 108, for example, at every 100 $\mu$ m, a force deforms each end portion of the conductive layers 103, 104 and 108 approximately 80 nm (i.e., 40% of the diameter). This means that the force is suppressed equal to approximately 1/10 of the case where the second opening portions 111 are not formed. If the deformation is approximately 40% of the diameter, connection at the first opening portions 107 may be maintained. In the present embodiment, it is considered that 10% order or approximately 100 $\mu$ m is the limit and the second opening portions 111 are formed at the distance  $L_1$  so as to be less than the limit. If the second opening portions 111 are not formed like the design in the related art, the entire force to deform the connection portions due to the changes in the wiring length of the third conduction layer 108 is applied to the connection portions at the first opening portions 107. However, forming the plural second opening portions 111, which do not contribute electrical connection, between the plural first opening portions 107 along the third conductive layer 108 helps to disperse the force resulting from the change in the wiring length and to be applied to the first opening portions 107. The predetermined distance  $L_1$  forming the first opening portions 107 and the second

opening portions 111 is not restricted to the present embodiment and may be changed depending on the material and film thickness of the conductive layers, the diameter of the opening portions, and the material and film thickness of the insulation film.

5      **【0039】**

          In the present embodiment, the first conductive layer and the second conductive layer are electrically connected to the third conductive layer by way of the first opening portions and the second opening portions which do not contribute electrical connection are formed between the plural first opening portions at a predetermined distance along the third conductive layer. As a result, any change in the wiring length in the direction of the longer length of the third conductive layer due to thermal expansion or contraction in the subsequent fabrication steps is dispersed, thereby suppressing deformation of the first opening portions. Accordingly, it prevents peeling of the connection portions from the bottom of the first opening portions formed at both end portions of the third conductive layer which defines the connection portions of the conductive layers. Therefore, production yield and wiring reliability are improved.

25      **【0040】**

          <Second Embodiment>

          Next, a fabrication method of a second embodiment of the semiconductor device according to the present invention will be described hereunder. It is to be noted that the same reference numerals as in the first embodiment are used to refer like elements, and no

description will be given thereon and description will be made herein on only different portions. FIG. 7 is a diagrammatic cross section view of the semiconductor device according to the second embodiment of the present invention. An insulation film 102 is formed on the upper surface of the semiconductor substrate 101. A plurality of wiring grooves 120 is formed at parts on the upper surface of the insulation film 102 at a predetermined distance. Formed alternately in the wiring grooves 120 are a first conductive layer 103 and a second conductive layer 104 at a predetermined distance. The first conductive layers 103 and the second conductive layers 104 are made from, for example, Cu. A diffusion protection film 105 is formed in such a manner to cover the first conductive layers 103 and the second conductive layers 104. Formed on the upper surface of the diffusion protection film 105 is an insulation film 106 which is made from allyl ether resin or the like having low Young's modulus. Wiring grooves 125 are formed on the upper surface of the insulation film 106. A third conductive layers 108 each having a predetermined wiring length  $L_2$  are formed in the wiring grooves 125. A diffusion protection film 109 and an insulation film 110 are sequentially formed on the upper surface of the insulation film 106 on which the third conductive layers 108 are formed. Incidentally, the third conductive layers 108 may be made from, for example, Cu. Each of the third conductive layers 108 having the wiring length  $L_2$  is electrically connected to the first conductive layers 103 at one end thereof and to the second conductive layers 104 at the other end by way of the opening portions 112.

The opening portions 112 are filled with the same material as the third conductive layers 108. It is to be noted that no device areas, device isolation areas and the like are shown in the drawing for simplifying the description.

5    **【0041】**

Next, the method of fabricating the semiconductor device according to the present invention will be described hereunder by reference to FIG. 8 and FIG. 9. FIG. 8 and FIG. 9 show diagrammatic cross section views for sequentially illustrating major steps of fabricating the semiconductor device according to the present invention. As shown in FIG. 8A, the insulation film 102 is formed on the upper surface of the semiconductor substrate 101 at the location where a predetermined device area is defined. A plurality of wiring grooves 120 each having the depth of approximately 200 nm are formed at the conductive layer forming area on the upper surface of the insulation film 102 at a predetermined distance from each other by the existing lithography process, etching process and the like. A 10 nm thick Ta film is formed as a barrier metal on the upper surface of the insulation film 102 on which the wiring grooves 120 are formed. An 80 nm thick Cu seed film and a 700 nm thick Cu film are formed as a first metal layer on the upper surface of the barrier metal 121. Subsequently, the first metal layer is polished by the CMP process or the like until the insulation film 102 is exposed and the first conductive layers 103 and the second conductive layers 104 are formed in the wiring grooves 120. In this present embodiment, although the first conductive layers 103 and the second conductive layers 104 are made from the same

metal layer, they may be made from different metal layers. It is to be noted that the barrier metal is not shown in the drawings and the first metal layer is shown as the first conductive layers 103 and the second conductive  
5 layers 104.

【0042】

Then, as shown in FIG. 8B, a 50 nm thick SiC film is formed as a diffusion protection film 105 for preventing the first conductive layers 103 and the second  
10 conductive layers 104 from diffusing. And an insulation film 106 made from allyl ether resin or the like having low Young's modulus is formed to have a thickness of approximately 600 nm. An appropriate method is employed for forming the diffusion protection film 105 and the  
15 insulation film 106 depending on materials of these films. It is to be noted that these films may be omitted depending on materials of the diffusion protection film 105 and the conductive layers 103, 104. Subsequently, the opening portions 112 are formed in the insulation film  
20 106 at end portions of each of the first conductive layers 103 and the second conductive layers 104 by the existing lithograph process and etching process. At this time, it is preferable that the diffusion protection film is left at the bottom of the opening portions 112.

25 【0043】

Subsequently, as shown in FIG. 9A, a buried layer is formed on the upper surface of the insulation film 106 in such a manner to fill up the opening portions 112. And a resist film is formed on the upper surface of the  
30 buried layer in a predetermined pattern to expose areas where the wiring grooves 125 are formed for the third



conductive layers 108 by the existing lithography process. The buried layer and the resist film are omitted in the drawing. Then, the existing etching technique is used to process the buried layer and the insulation film 106 at the areas where the resist film is not formed. Subsequently, the resist film and the buried layer are removed to form approximately 300 nm deep wiring grooves 125 having the predetermined length  $L_2$ . Furthermore, the diffusion protection film 105 exposed to the opening portions 112 is removed by etching process or the like, thereby exposing the first conductive layers 103 and the second conductive layers 104.

【0044】

Subsequently, in FIG. 9B, an approximately 20 nm thick Ta film is formed as the barrier metal on the upper surface of the insulation film 106 where the opening portions 112 and the wiring grooves 125 are formed. Also formed is a metal layer which includes an approximately 80 nm thick Cu seed film and an approximately 800 nm thick Cu film. Polishing is performed by the CMP process or the like until the insulation film 106 is exposed, thereby forming the third conductive layers 108 each having a predetermined length  $L_2$  in the wiring grooves 125. The material of the third conductive layers 108 is not limited to the one as described hereinabove but may be any other conductive material containing Cu. In the drawing, the barrier metal is omitted and the third conductive layers 108 are only shown as the second metal layer. Then, in the same process as described hereinabove, the diffusion protection film 109 and the insulation film 109 are formed. If necessary, conductive layers and the like are further

formed to complete the multi-layer wiring as shown in FIG. 7.

【0045】

In the present embodiment as shown in FIG. 7, the  
5 predetermined wiring length  $L_2$  of the third conductive  
layers 108 is set to, for example, approximately  $100\mu\text{m}$ .  
Each of the third conductive layers 108 has a pair of  
opening portions 112 at both ends. One of the opening  
portions makes electrical connection with the first  
10 conductive layers 103 while the other opening portion  
makes electrical connection with the second conductive  
layers 104. In this configuration, the first conductive  
layers 103 are electrically connected to different third  
conductive layers 108 at the both ends thereof while the  
15 second conductive layers 104 are electrically connected  
to different third conductive layers 108 at both ends  
thereof. Such configuration may be repeated. It is to  
be noted that allyl ether resin is used as the insulation  
film 106 in which the opening portions 112 are formed  
20 for making connection between the third conductive layers  
108 and the underlying first and second conductive layers  
103, 104, wherein these conductive layers are made from  
Cu. At this time, Young's modulus and coefficient of  
thermal expansion of Cu are 115 Gpa and  $17.7\text{ ppm}/^\circ\text{C}$  while  
25 those of allyl ether resin are  $2.45\text{ Gpa}$  and  $66\text{ ppm}/^\circ\text{C}$ ,  
respectively. For example, assuming that the wiring  
length  $L_2$  of the conductive layers 103, 104 and 108 is  
approximately  $1000\mu\text{m}$  (repetitive configuration of  $1000\mu\text{m}$   
long upper conductive layers and  $1000\mu\text{m}$  long lower  
30 conductive layers) and that the insulation film 106 made  
from allyl ether resin is formed between the upper

conductive layer and the lower conductive layer. If the semiconductor device is actually used at the temperature of approximately 100°C, the aforementioned Young's modulus and coefficient of thermal expansion suggest that  
5 the end portions of the conductive layers expand approximately 800 nm per end. In other words, forces are applied from the lower conductive layers 103, 104 to the opening portions 112 to deform 800 nm in one direction and from the upper conductive layers 108 to  
10 deform 800 nm in the opposite direction.

【0046】

In view of the 130 nm generation, since the diameter of the opening portions 112 is approximately 200 nm, a force enabling to deform the diameter equal to  
15 approximately 400% in the wiring length direction of the wiring, each in the opposite directions from the upper layer and the lower layer. Accordingly, since the opening portions 112 and the underlying conductive layers 103, 104 at the bottom portion of the opening portions  
20 112 are connected with insufficient adherence by way of the barrier metal, it is easily understood that disconnection may occur. In the case where the wiring length  $L_2$  of the third conductive layers 108 is set to, for example, 100  $\mu\text{m}$ , a deforming force to be applied to  
25 each end of the conductive layers is only approximately 80 nm (i.e., 40% of the diameter), thereby reducing the force to approximately 1/10 of the case having the wiring length equal to 1000  $\mu\text{m}$ . If the deformation is in the order of approximately 40% of the diameter, connection  
30 at the opening portions 112 may be maintained. In the present embodiment of the present invention, it is

considered that 10% order or approximately  $100\mu\text{m}$  is the limit, so that the third conductive layers 108 are formed so as to have the wiring length  $L_2$  equal to or less than such a limit. In case of making electrical connection  
5 by the opening portions at both ends of a long conductive layer like the design in the related art, the entire force to deform the connection portion due to thermal expansion of the conductive layer is applied to the opening portions, thereby increasing the possibility of peeling the  
10 connection portions. On the contrary, by forming the third conductive layers 108 each having a predetermined wiring length  $L_2$  in such a manner to maintain the connection at the opening portions even if the conductive layer of the third conductive layers 108 may thermally  
15 expand or contract, the force to be applied to the opening portions caused by thermal expansion or contraction of the wiring length can be reduced.

【0047】

It is to be noted that the wiring length  $L_2$  of the  
20 third conductive layers 108 is not restricted to the present embodiment but may vary depending on the material and thickness of the conductive layers, the diameter of the opening portions and the material and film thickness of the insulation film. It is preferable that the wiring  
25 length of the first conductive layers 103 and the second conductive layers 104 is substantially equal to the wiring length  $L_2$  of the third conductive layers 108 if the first conductive layers 103 and the second conductive layers 104 are made from the same material as the third conductive  
30 layers 108. Furthermore, if the wiring length is calculated from Young's modulus and coefficient of

thermal expansion of the material forming the conductive layer of the first conductive layers 103 and the second conductive layers 104 in the same manner as the above, the force applied from the lower layer electrodes is  
5 further reduced.

【0048】

In the present embodiment of the present invention, by restricting the wiring of the third conductive layers to a predetermined length, peeling of the connection  
10 portions due to change of the wiring length in the direction of the longer length resulting from thermal expansion or contraction is suppressed, thereby preventing deformation of the opening portions and maintaining the electrical connection. As a result,  
15 production yield and wiring reliability of the semiconductor device are significantly improved.

【0049】

It is to be noted that the present invention should not be restricted only to the above embodiments. For  
20 example, in the first embodiment, the distance of the second opening portions formed between the first opening portions can be changed depending on the thickness of the conductive layer, the diameter of the opening portions and the like. On the other hand, in the second embodiment,  
25 the wiring length of the third conductive layers may be changed depending on the thickness of the conductive layers and material of the insulation film. It is also understood that various other changes and modifications can be made without departing from the scope of the present  
30 invention.